UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
08/699,844	08/20/1996	DAVID R. DETTMER	18799.79(TT1	3703

7590 10/07/2004

CRAWFORD PLLC
1270 NORTHLAND DRIVE
SUITE 390
MENDOTA HEIGHTS, MN 55120

EXAMINER	
SWERDLOW, DANIEL	
ART UNIT	**PAPER NUMBER**
2644	

DATE MAILED: 10/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No.	Applicant(s)	
	08/699,844	DETTMER, DAVID R.	
	Examiner	Art Unit	
	Daniel Swerdlow	2644	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 30 August 2004 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☐ The period for reply expires _____months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2. ☐ The proposed amendment(s) will not be entered because:

   (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);

   (b) ☐ they raise the issue of new matter (see Note below);

   (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

   (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____.

3. ☐ Applicant's reply has overcome the following rejection(s): _____.

4. ☒ Newly proposed or amended claim(s) *29-31 and 33-35* would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5. ☐ The a)☐ affidavit, b)☐ exhibit, or c)☐ request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.

6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7. ☐ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:

   Claim(s) allowed: _____.

   Claim(s) objected to: _____.

   Claim(s) rejected: _____.

   Claim(s) withdrawn from consideration: _____.

8. ☐ The drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9. ☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10. ☒ Other: *See attached*

DETAILED ACTION

The after final amendment filed on 30 August 2004 is entered. As a result, Claims 29 through 31 and 33 through 35 are allowable. Claims 1, 2, 4, 7 through 9, 24 through 28 and 32 are rejected for reasons stated in the prior Office action.

Response to Arguments

1. Applicant's arguments filed 30 August 2004 have been fully considered but they are not persuasive.

2. In the first complete paragraph on page 10 of the response filed on 30 August 2004, applicant alleges that the IIR peak detectors disclosed by McCaslin do not correspond to the hands-free receive register and the hands-free transmit register claimed. Examiner respectfully disagrees. The terms "hands-free receive register" and "hands-free transmit register" are neither terms of art nor explicitly defined in the disclosure. The IIR peak detectors disclosed by McCaslin are used in a speakerphone (Fig. 19), which is a hands-free device. Further, McCaslin discloses one IIR peak detector to operate on the received signal (Fig. 20, reference 420) and another to operate on the transmitted signal (Fig. 20, reference 428). Further, the IIR peak detector that operates on the received signal (Fig. 20, reference 420) has as its input the signal Rin(k), which is the output of an analog to digital converter (Fig. 1, reference 12). Similarly, the IIR peak detector that operates on the Transmitted signal (Fig. 20, reference 428) has as its input the signal Sin(k), which is the output of an analog to digital converter (Fig. 19, reference 34). As such, each of the IIR peak detectors disclosed by McCaslin is coupled to an analog to digital converter as claimed. Further, as shown by Fig. 20, each of the IIR peak detectors disclosed by McCaslin is coupled to processing steps that correspond to the microprocessor claimed. Finally,

a register is "a device (as in a computer) for storing small amounts of data; esp : one in which data can be both stored and operated on" (Webster's Ninth New Collegiate Dictionary, Merriam-Webster, 1990). An IIR filter, which mathematically combines new input data with a previous result, meets this definition. As such, the IIR peak detectors disclosed by McCaslin correspond to the "hands-free receive register" and "hands-free transmit register" claimed.

3. In the second complete paragraph on page 10 of the response filed on 30 August 2004, applicant alleges that examiner has made mutually contradictory statements regarding the teaching of McCaslin relating to the alternate reception of signals in the respective speech paths. Examiner respectfully disagrees. Alternate reception of signals in the respective speech paths is taught by McCaslin. McCaslin teaches "input of the far end signal Rin(k) to the peak detect IIR filter 420" (column 22, lines 6-7) and "the near end transmit power Sin(k) is input to a peak detector IIR filter 428" (column 22, lines 36-37). Since the same index, k, is used for both inputs, it is clear that each quantity is received each input period. As such, the inputs are received alternately. This is not contradicted by the statement that in the combination of McCaslin and Barron, the microprocessor alternately receives the signals.

4. In the paragraph spanning pages 10 and 11 of the response filed on 30 August 2004, applicant alleges: "If both signals are received for each sample, then the asserted alternate receipt of the two signals would negate such simultaneous receipt as half of the sampled near end and far end signals would be ignored due to the alternate receipt by the microprocessor. Alternating receipt of the two signals would mean that only one of the signals (near end or far end) would be received at each sample time, as the two signals are alleged to be sampled together." Examiner respectfully disagrees. There is no reason why both signals cannot be

alternately received without skipping any samples of either signal as long as the signals are processed at a rate at least twice the sampling rate of the signals. Since the sampling rate is 8,000 samples per second and typical processing rates at the time of the invention were in the tens of millions of cycles per second, there is ample time to alternately receive every sample of both signals.

5. In the first complete paragraph on page 11 of the response filed on 30 August 2004, applicant alleges: "This minimization would be inaccurate as half of the signals necessary for such a determination would not be received." Examiner respectfully disagrees. As shown above, the references cited do not teach skipping of samples.

6. In the paragraph spanning pages 11 and 12 of the response filed on 30 August 2004, applicant alleges that the implementation of the peak detection taught by McCaslin using an algorithm on a microprocessor taught by Barron would slow the operation of the speakerphone to the point of "frustrating the operation". Examiner respectfully disagrees. The disparity between telephone audio sampling rate and processor speed as described above makes clear that microprocessor-based algorithms can be applied to speakerphone processing.

7. In the first complete paragraph on page 12 of the response filed on 30 August 2004, applicant alleges: "The Examiner's response at page 17, paragraph 36, fails to account for the fact that the functional blocks of Fig. 19 are described using the discrete components of Fig. 1, which admittedly do not include a microprocessor (see Examiner's characterization of '794 Fig. 1 embodiment at page 4, paragraph 3, of the Office Action). It is well known in the electronic arts to implement such functional blocks with discrete components. For example, the top of page 8 of VHDL Made Easy! (enclosed) teaches a commonly-used approach for implementing

functional blocks by discrete hardware (logic circuit) components. The treatise further teaches how IEEE Standard 1164 is used for such implementations. The Examiner's rationale in this regard fails. Applicant maintains the previous position that the '794 reference does not teach use of a microprocessor and does not provide any evidence that would motivate the skilled artisan to modify it to do so. Without a presentation of correspondence to each of the claimed limitations, the Section 103(a) rejection is improper and should be withdrawn." Examiner respectfully disagrees. First, nowhere does McCaslin contain reference to any discrete components. Fig. 1, an embodiment not relied except to show the origins of the signals Rin(k) and Sin(k) for the embodiment of Figs. 19 and 20, shows a doubletalk detector and a finite impulse response adaptive filter, neither of which are discrete components. Similarly, Fig. 19 shows an echo suppressor (reference 414) as a functional block, not as discrete components and Fig. 20 shows a more detailed version of the echo suppressor of Fig. 19, again as a relationship among functional blocks (see column 22, lines 4-6 for the relationship of Figs. 19 and 20). Whether or not it is "well known in the electronic arts to implement such functional blocks with discrete components" is not relevant here since McCaslin makes no teaching one way or the other in that regard. McCaslin lays out functions and algorithms and leaves it to one skilled in the art to provide a physical implementation. As stated in the rejections in the prior Office action, one skilled in the art at the time of the invention (i.e., 20 August 1996) would have teaching from Barron that a microprocessor could be successfully used to set gain in the transmit and receive lines of a speakerphone and motivation to apply that teaching in order to practice the invention disclosed by McCaslin. Applicant's submission of selected pages from "VHDL Made Easy!" is considered irrelevant for the reasons stated above. Further, VHDL is a programming language

used to simulate the operation digital electronic systems. It is usable in designing microprocessors. Insofar as microprocessors comprise components (e.g., millions of transistors), VHDL is used to simulate the action of these components. However, the existence of such a programming language is not evidence of the unobviousness of using a microprocessor to implement the functions of a speakerphone.

Allowable Subject Matter

8. Applicant has rewritten Claims 29 through 31 and 33 through 35 in independent form including all of the limitations of the base claim and any intervening claims. The amendment has been entered. As such, these claims are allowable for reasons stated in the prior Office action.

ds

FORESTER W. ISEN
SUPERVISORY PATENT EXAMINER